DESCRIPTION

This is a family of 2097152-word by 8-bit dynamic RAMS, fabricated with the high performance CMOS process,and is ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential.

The use of double-layer aluminum process combined with triple-well CMOS technology and a single-transistor dynamic storage stacked capacitor cell provide high circuit density at reduced costs. Multiplexed address inputs permit both a reduction in pins and an increase in system densities.

FEATURES

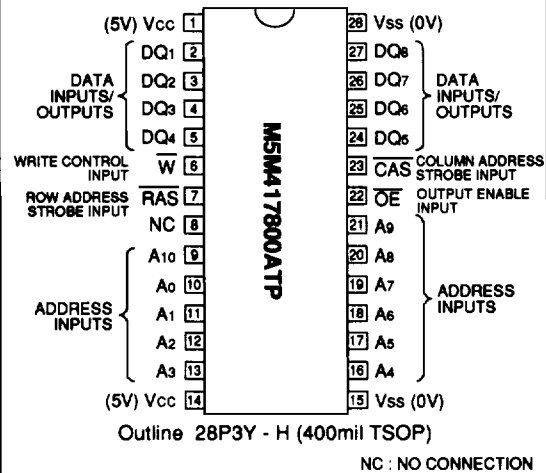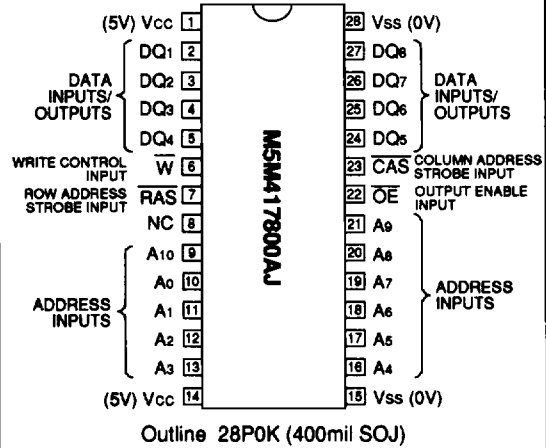| Type name	RAS access time (max.ns)	CAS access time (max.ns)	Address access time (max.ns)	OE access time (max.ns)	Cycle time (min.ns)	Power dissipation (typ.mW)
M5M417800AXX-6,-6S	60	15	30	15	110	540
M5M417800AXX-7,-7S	70	20	35	20	130	475

XX = J, TP

- Standard 28 pin SOJ, 28 pin TSOP
- Single 5V ± 10%supply
- Low stand-by power dissipation
  5.5mW (Max) ································· CMOS input level
  2.2mW*(Max) ································· CMOS input level
- Low operating power dissipation
  M5M417800Axx- 6, -6S ···················· 660.0mW (Max)
  M5M417800Axx- 7, -7S ···················· 580.0mW (Max)
- Self refresh capability *
  self refresh current ·················· 400.0μA (Max)
- Fast-page mode, Read-modify-write,RAS-only refresh, CAS before RAS refresh, Hidden refresh capabilities
- Early-write mode and OE to control output buffer impedance
- All inputs, output TTL compatible and low capacitance
- 2048 refresh cycles every 32ms (Ao~A10)
  *Applicable to self refresh version (M5M417800AJ, TP-6S, -7S : option only)

APPLICATION

Main memory unit for computers, Microcomputer memory, Refresh memory for CRT

PIN CONFIGURATION (TOP VIEW)

(5V) Vcc	1	28	Vss (0V)
DATA INPUTS/OUTPUTS { DQ1	2	27	DQ8 } DATA INPUTS/OUTPUTS
DQ2	3	26	DQ7
DQ3	4	25	DQ6
DQ4	5	24	DQ5
WRITE CONTROL INPUT W	6	23	CAS COLUMN ADDRESS STROBE INPUT
ROW ADDRESS STROBE INPUT RAS	7	22	OE OUTPUT ENABLE INPUT
NC	8	21	A9
ADDRESS INPUTS { A10	9	20	A8 } ADDRESS INPUTS
Ao	10	19	A7
A1	11	18	A6
A2	12	17	A5
A3	13	16	A4
(5V) Vcc	14	15	Vss (0V)

M5M417800AJ

Outline 28P0K (400mil SOJ)

(5V) Vcc	1	28	Vss (0V)
DATA INPUTS/OUTPUTS { DQ1	2	27	DQ8 } DATA INPUTS/OUTPUTS
DQ2	3	26	DQ7
DQ3	4	25	DQ6
DQ4	5	24	DQ5
WRITE CONTROL INPUT W	6	23	CAS COLUMN ADDRESS STROBE INPUT
ROW ADDRESS STROBE INPUT RAS	7	22	OE OUTPUT ENABLE INPUT
NC	8	21	A9
ADDRESS INPUTS { A10	9	20	A8 } ADDRESS INPUTS
Ao	10	19	A7
A1	11	18	A6
A2	12	17	A5
A3	13	16	A4
(5V) Vcc	14	15	Vss (0V)

M5M417800ATP

Outline 28P3Y - H (400mil TSOP)

NC : NO CONNECTION

FUNCTION

The M5M417800AJ, TP provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., fast page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown in Table 1.

Table 1 Input conditions for each mode

Operation	Inputs						Input/Output		Refresh	Remark
	$\overline{RAS}$	$\overline{CAS}$	$\overline{W}$	$\overline{OE}$	Row address	Column address	Input	Output		
Read	ACT	ACT	NAC	ACT	APD	APD	OPN	VLD	YES	
Write (Early write)	ACT	ACT	ACT	DNC	APD	APD	VLD	OPN	YES	Fast page mode identical
Write (Delayed write)	ACT	ACT	ACT	DNC	APD	APD	VLD	IVD	YES	
Read-modify-write	ACT	ACT	ACT	ACT	APD	APD	VLD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	DNC	OPN	YES	
Hidden refresh	ACT	ACT	DNC	ACT	APD	DNC	OPN	VLD	YES	
Self refresh	ACT	ACT	DNC	DNC	DNC	DNC	DNC	OPN	YES	
$\overline{CAS}$ before $\overline{RAS}$ refresh	ACT	ACT	NAC	DNC	DNC	DNC	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active, NAC : nonactive, DNC : don' t care, VLD : valid, IVD : invalid, APD : applied, OPN : open

BLOCK DIAGRAM
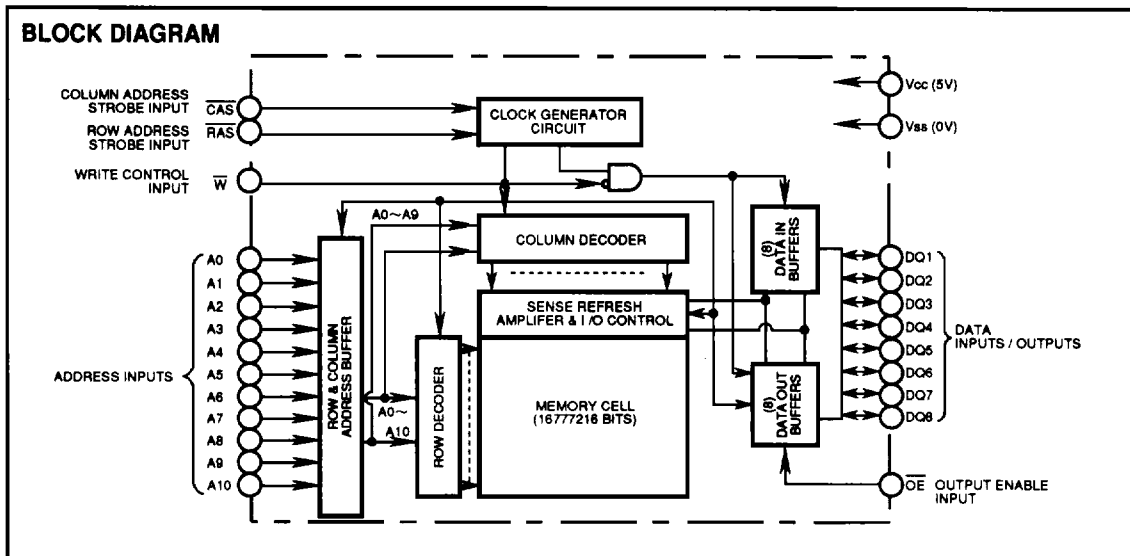
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage		−1∼7	V
Vi	Input voltage	With respect to Vss	−1∼7	V
Vo	Output voltage		−1∼7	V
Io	Output current		50	mA
Pd	Power dissipation	Ta = 25℃	1000	mW
Topr	Operating temperature		0∼70	℃
Tstg	Storage temperature		−65∼150	℃

RECOMMENDED OPERATING CONDITIONS (Ta = 0∼70℃, unless otherwise noted) (Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
Vcc	Supply voltage	4.5	5	5.5	V
Vss	Supply voltage	0	0	0	V
VIH	High-level input voltage, all inputs	2.4		6.0	V
VIL	Low-level input voltage, all inputs	−1.0		0.8	V

Note 1 : All voltage values are with respect to Vss

ELECTRICAL CHARACTERISTICS (Ta = 0∼70℃, Vcc = 5V±10%, Vss = 0V, unless otherwise noted) (Note 2)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
VOH	High-level output voltage		IOH = −5mA	2.4		Vcc	V
VOL	Low-level output voltage		IOL = 4.2mA	0		0.4	V
Ioz	Off-state output current		Q floating 0V≦VOUT≦5.5V	−10		10	μA
Ii	Input current		0V≦VIN≦6.5V, Other inputs pins = 0V	−10		10	μA
ICC1 (AV)	Average supply current from Vcc operating (Note 3,4)	M5M417800A-6,-6S	$\overline{RAS}$, $\overline{CAS}$ cycling tRC = tWC = min. output open			120	mA
		M5M417800A-7,-7S				105	
ICC2	Supply current from Vcc , stand-by		$\overline{RAS}$ = $\overline{CAS}$ =VIH, output open			2	mA
			$\overline{RAS}$ = $\overline{CAS}$≧Vcc -0.5			1	
ICC3 (AV)	Average supply current from Vcc refreshing (Note 3)	M5M417800A-6,-6S	$\overline{RAS}$ cycling, $\overline{CAS}$ = VIH tRC = min. output open			120	mA
		M5M417800A-7,-7S				105	
ICC4 (AV)	Average supply current from Vcc Fast-Page-Mode (Note 3,4)	M5M417800A-6,-6S	$\overline{RAS}$ = VIL, $\overline{CAS}$ cycling tPC = min. output open			70	mA
		M5M417800A-7,-7S				60	
ICC6 (AV)	Average supply current from Vcc $\overline{CAS}$ before $\overline{RAS}$ refresh mode (Note 3)	M5M417800A-6,-6S	$\overline{CAS}$ before $\overline{RAS}$ refresh cycling tRC = min. output open			120	mA
		M5M417800A-7,-7S				105	

Note 2: Current flowing into an IC is positive, out is negative.
3: ICC1 (AV), ICC3 (AV), ICC4 (AV) and ICC6 (AV) are dependent on cycle rate. Maximum current is measured at the fastest cycle rate.
4: ICC1 (AV) and ICC4 (AV) are dependent on output loading. Specified values are obtained with the output open.

CAPACITANCE (Ta = 0∼70℃, Vcc = 5V±10%, Vss = 0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
CI (A)	Input capacitance, address inputs				5	pF
CI (OE)	Input capacitance, $\overline{OE}$ input				7	pF
CI (W)	Input capacitance, write control input	VI = Vss			7	pF
CI (RAS)	Input capacitance, $\overline{RAS}$ input	f = 1MHz			7	pF
CI (CAS)	Input capacitance, $\overline{CAS}$ input	VI = 25mVrms			7	pF
CI/O	Input/Output capacitance, data ports				8	pF

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SWITCHING CHARACTERISTICS (Ta = 0~70°C, Vcc = 5V±10%, Vss = 0V, unless otherwise noted, see notes 5,12,13)

Symbol	Parameter		Limits				Unit
			M5M417800A-6,-6S		M5M417800A-7,-7S		
			Min	Max	Min	Max	
tCAC	Access time from $\overline{CAS}$	(Note 6,7)		15		20	ns
tRAC	Access time from $\overline{RAS}$	(Note 6,8)		60		70	ns
tAA	Columu address access time	(Note 6,9)		30		35	ns
tCPA	Access time from $\overline{CAS}$ precharge	(Note 6,10)		35		40	ns
tOEA	Access time from $\overline{OE}$	(Note 6)		15		20	ns
tCLZ	Output low impedance time from $\overline{CAS}$ low	(Note 6)	5		5		ns
tOFF	Output disable time after $\overline{CAS}$ high	(Note 11)	0	15	0	15	ns
tOEZ	Output disable time after $\overline{OE}$ high	(Note 11)	0	15	0	15	ns

Note 5 : An initial pause of 500 μ s is required after power-up followed by a minimum of eight initialization cycles (any combination of cycles containing a $\overline{RAS}$ clock such as $\overline{RAS}$-Only refresh).
Note the $\overline{RAS}$ may be cycled during the initial pause. And any 8 $\overline{RAS}$ or $\overline{RAS}/\overline{CAS}$ cycles are required after prolonged periods (greater than 32 ms) of $\overline{RAS}$ inactivity before proper device operation is achieved.

6 : Measured with a load circuit equivalent to 2TTL loads and 100pF.

7 : Assumes that tRCD≧tRCD (max) and tASC≧tASC (max).

8 : Assumes that tRCD≦tRCD (max) and tRAD≦tRAD (max). If tRCD or tRAD is greater than the maximum recommended value shown in this table, tRAC will increase by amount that tRCD exceeds the value shown.

9 : Assumes that tRAD≧tRAD (max) and tASC≦tASC (max).

10 : Assumes that tCP≦tCP (max) and tASC≧tASC (max).

11 : tOFF (max) and tOEZ (max) defines the time at which the output achieves the high impedance state (Iout≦I±10 μ Al) and is not reference to VOH (min) or VOL (max).

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Fast-Page Mode Cycles)
(Ta = 0~70°C, Vcc = 5V±10%, Vss = 0V, unless otherwise noted See notes 12,13)

Symbol	Parameter		Limits				Unit
			M5M417800A-6,-6S		M5M417800A-7,-7S		
			Min	Max	Min	Max	
tREF	Refresh cycle time			32		32	ms
tRP	$\overline{RAS}$ high pulse width		40		50		ns
tRCD	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low	(Note14)	20	45	20	50	ns
tCRP	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low		10		10		ns
tRPC	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low		0		0		ns
tCPN	$\overline{CAS}$ high pulse width		10		10		ns
tRAD	Column address delay time from $\overline{RAS}$ low	(Note15)	15	30	15	35	ns
tASR	Row address setup time before $\overline{RAS}$ low		0		0		ns
tASC	Column address setup time before $\overline{CAS}$ low	(Note16)	0	10	0	10	ns
tRAH	Row address hold time after $\overline{RAS}$ low		10		10		ns
tCAH	Column address hold time after $\overline{CAS}$ low		15		15		ns
tDZC	Delay time, data to $\overline{CAS}$ low	(Note17)	0		0		ns
tDZO	Delay time, data to $\overline{OE}$ low	(Note17)	0		0		ns
tCDD	Delay time, $\overline{CAS}$ high to data	(Note18)	15		15		ns
tODD	Delay time, $\overline{OE}$ high to data	(Note18)	15		15		ns
tT	Transition time	(Note19)	1	50	1	50	ns

Note 12 : The timing requirements are assumed tT =5ns.

13 : VIH (min) and VIL (max) are reference levels for measuring timing of input signals.

14 : tRCD (max) is specified as a reference point only. If tRCD is less than tRCD (max), access time is tRAC. If tRCD is greater than tRCD (max), access time is controlled exclusively by tCAC or tAA. tRCD (min) is specified as tRCD (min) = tRAH (min) + 2tH + tASC (min).

15 : tRAD (max) is specified as a reference point only. If tRAD ≧ tRAD (max) and tASC ≦ tASC (max), access time is controlled exclusively by tAA.

16 : tASC (max) is specified as a reference point only. If tRCD ≧ tRCD (max) and tASC ≧ tASC (max), access time is controlled exclusively by tCAC.

17 : Either tDZC or tDZO must be satisfied.

18 : Either tCDD or tODD must be satisfied.

19 : tT is measured between VIH (min) and VIL (max).

Read and Refresh Cycles

Symbol	Parameter		Limits				Unit
			M5M417800A-6,-6S		M5M417800A-7,-7S		
			Min	Max	Min	Max	
tRC	Read cycle time		110		130		ns
tRAS	RAS low pulse width		60	10000	70	10000	ns
tCAS	CAS low pulse width		15	10000	20	10000	ns
tCSH	CAS hold time after RAS low		60		70		ns
tRSH	RAS hold time after CAS low		15		20		ns
tRCS	Read Setup time after CAS high		0		0		ns
tRCH	Read hold time after CAS low	(Note 20)	0		0		ns
tRRH	Read hold time after RAS low	(Note 20)	10		10		ns
tRAL	Column address to RAS hold time		30		35		ns
tOCH	CAS hold time after OE low		15		20		ns
tORH	RAS hold time after OE low		15		20		ns

Note 20 : Either tRCH or tRRH must be satisfied for a read cycle.

Write Cycle (Early Write and Delayed Write)

Symbol	Parameter		Limits				Unit
			M5M417800A-6,-6S		M5M417800A-7,-7S		
			Min	Max	Min	Max	
tWC	Write cycle time		110		130		ns
tRAS	RAS low pulse width		60	10000	70	10000	ns
tCAS	CAS low pulse width		15	10000	20	10000	ns
tCSH	CAS hold time after RAS low		60		70		ns
tRSH	RAS hold time after CAS low		15		20		ns
tWCS	Write setup time before CAS low	(Note 22)	0		0		ns
tWCH	Write hold time after CAS low		10		10		ns
tCWL	CAS hold time after W low		15		20		ns
tRWL	RAS hold time after W low		15		20		ns
tWP	Write pulse width		10		10		ns
tDS	Data setup time before CAS low or W low		0		0		ns
tDH	Data hold time after CAS low or W low		10		15		ns
tOEH	OE hold time after W low		15		20		ns

Read-Write and Read-Modify-Write Cycles

Symbol	Parameter		Limits				Unit
			M5M417800A-6,-6S		M5M417800A-7,-7S		
			Min	Max	Min	Max	
tRWC	Read write/read modify write cycle time	(Note21)	155		180		ns
tRAS	$\overline{RAS}$ low pulse width		105	10000	120	10000	ns
tCAS	$\overline{CAS}$ low pulse width		60	10000	70	10000	ns
tCSH	$\overline{CAS}$ hold time after $\overline{RAS}$ low		105		120		ns
tRSH	$\overline{RAS}$ hold time after $\overline{CAS}$ low		60		70		ns
tRCS	Read setup time before $\overline{CAS}$ low		0		0		ns
tCWD	Delay time, $\overline{CAS}$ low to $\overline{W}$ low	(Note22)	40		45		ns
tRWD	Delay time, $\overline{RAS}$ low to $\overline{W}$ low	(Note22)	85		95		ns
tAWD	Delay time, address to $\overline{W}$ low	(Note22)	55		60		ns
tCWL	$\overline{CAS}$ hold time after $\overline{W}$ low		15		20		ns
tRWL	$\overline{RAS}$ hold time after $\overline{W}$ low		15		20		ns
tWP	Write pulse width		10		10		ns
tDS	Data setup time before $\overline{W}$ low		0		0		ns
tDH	Data hold time after $\overline{W}$ low		10		15		ns
tOEH	$\overline{OE}$ hold time after $\overline{W}$ low		15		15		ns

Note 21 : tRWC is specified as tRWC (min) = tRAC (max) + tODD (min) + tRWL (min) + tRP (min) + 5tT.
22 : twcs, tcwd, tRWD and tAWD and, tCPWD are specified as reference points only. If twcs≧twcs (min) the cycle is an early write cycle and the
DQ pins will remain high impedance throughout the entire cycle. If tCWD≧tCWD(min), tRWD≧tRWD (min), tAWD≧tAWD (min) and tCPWD≧tCPWD (min)
(for fast page mode cycle only), the cycle is a read-modify-write cycle and the DQ will contain the data read from the selected address.
If neither of the above condition (delayed write) of the DQ (at access time and until $\overline{CAS}$ or $\overline{OE}$ goes back to VIH) is indeterminate.

Fast-Page Mode Cycle (Read, Early Write, Read -Write, Read-Modify-Write Cycle) (Note 23)

Symbol	Parameter		Limits				Unit
			M5M417800A-6,-6S		M5M417800A-7,-7S		
			Min	Max	Min	Max	
tPC	Fast page mode read/write cycle time		40		45		ns
tPRWC	Fast page mode read write/read modify write cycle time		85		95		ns
tRAS	$\overline{RAS}$ low pulse width for read write cycle	(Note24)	100	125000	115	125000	ns
tCP	$\overline{CAS}$ high pulse width	(Note25)	10	15	10	15	ns
tCPRH	$\overline{RAS}$ hold time after $\overline{CAS}$ precharge		35		40		ns
tCPWD	Delay time, $\overline{CAS}$ precharge to $\overline{W}$ low	(Note22)	60		65		ns

Note 23 : All previously specified timing requirements and switching characteristics are applicable to their respective fast page mode cycle.
24 : tRAS (min) is specified as two cycles of $\overline{CAS}$ input are performed.
25 : tCP (max) is specified as a reference point only.

$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle (Note 26)

Symbol	Parameter	Limits				Unit
		M5M417800A-6,-6S		M5M417800A-7,-7S		
		Min	Max	Min	Max	
tCSR	$\overline{CAS}$ setup time before $\overline{RAS}$ low	10		10		ns
tCHR	$\overline{CAS}$ hold time after $\overline{RAS}$ low	10		15		ns
tRSR	Read setup time before $\overline{RAS}$ low	10		10		ns
tRHR	Read hold time after $\overline{RAS}$ low	10		15		ns

Note 26 : Eight or more $\overline{CAS}$ before $\overline{RAS}$ cycles instead of eight $\overline{RAS}$ cycles are necessary for proper operation of $\overline{CAS}$ before $\overline{RAS}$ refresh mode.

Timing Diagrams (Note 27)
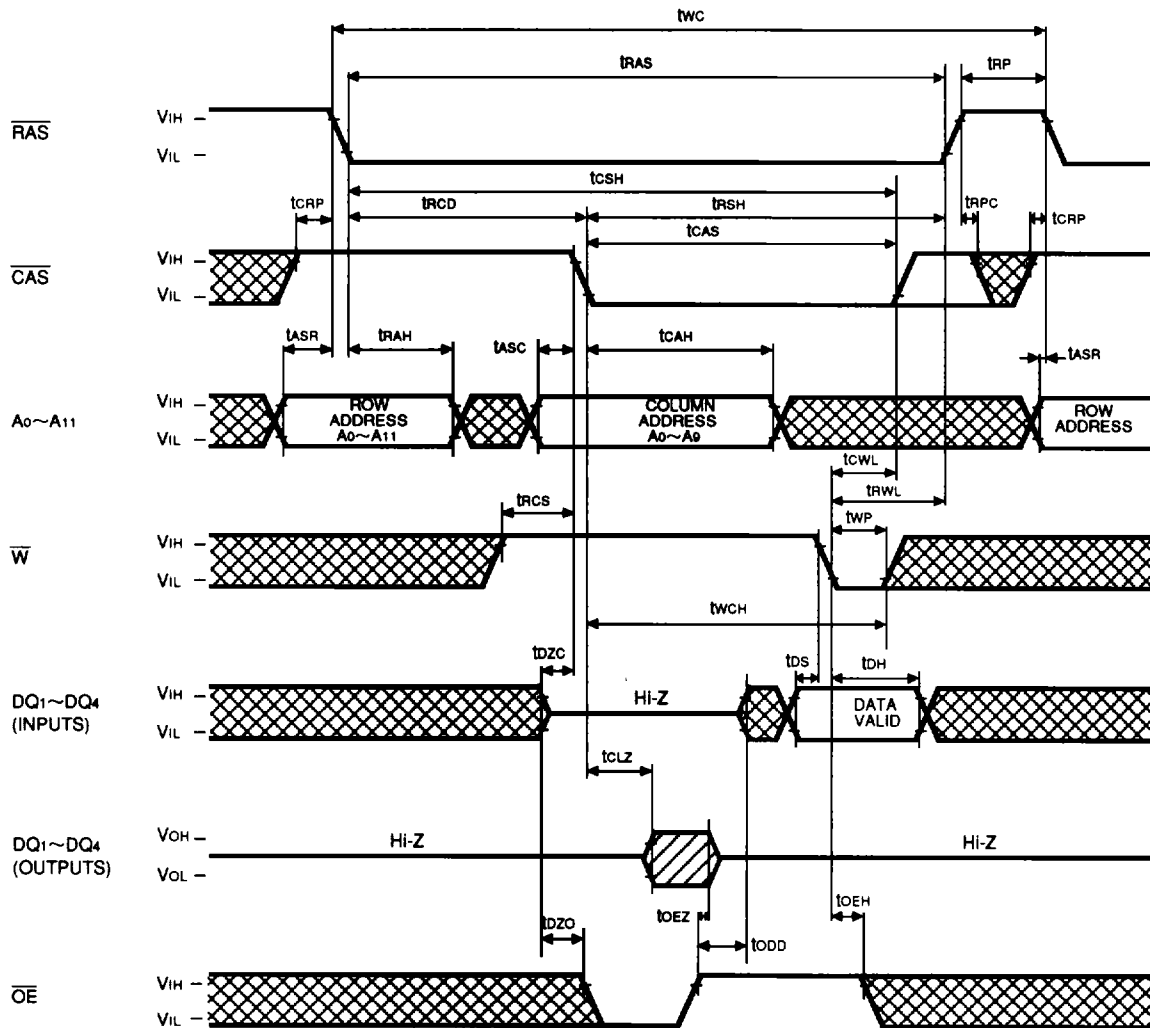### Read Cycle
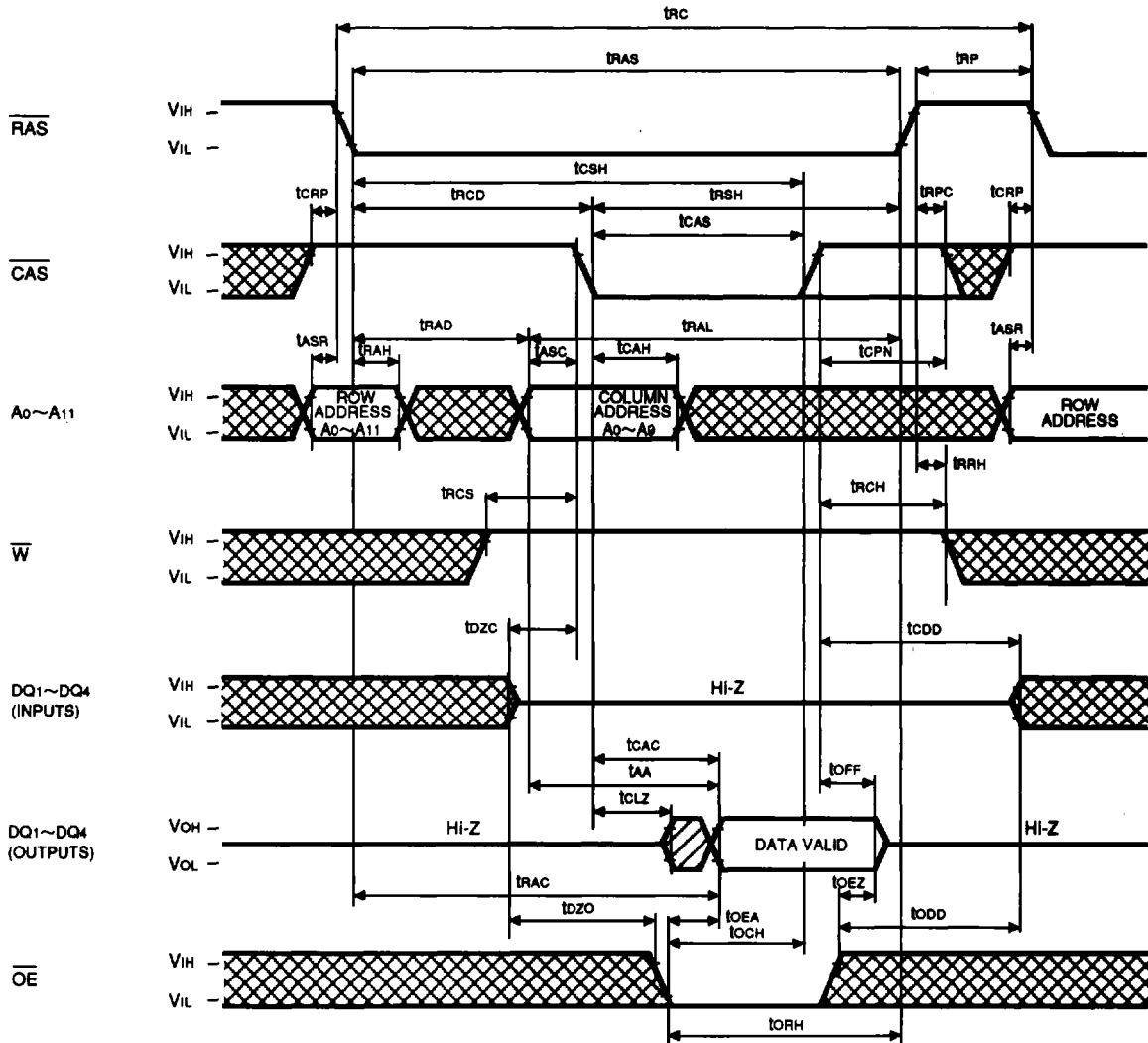
Note 27

Indicates the don't care input.
$V_{IH}(min) \leq V_{IN} \leq V_{IH}(max)$ or $V_{IL}(min) \leq V_{IN} \leq V_{IL}(max)$

Indicates the invalid output.

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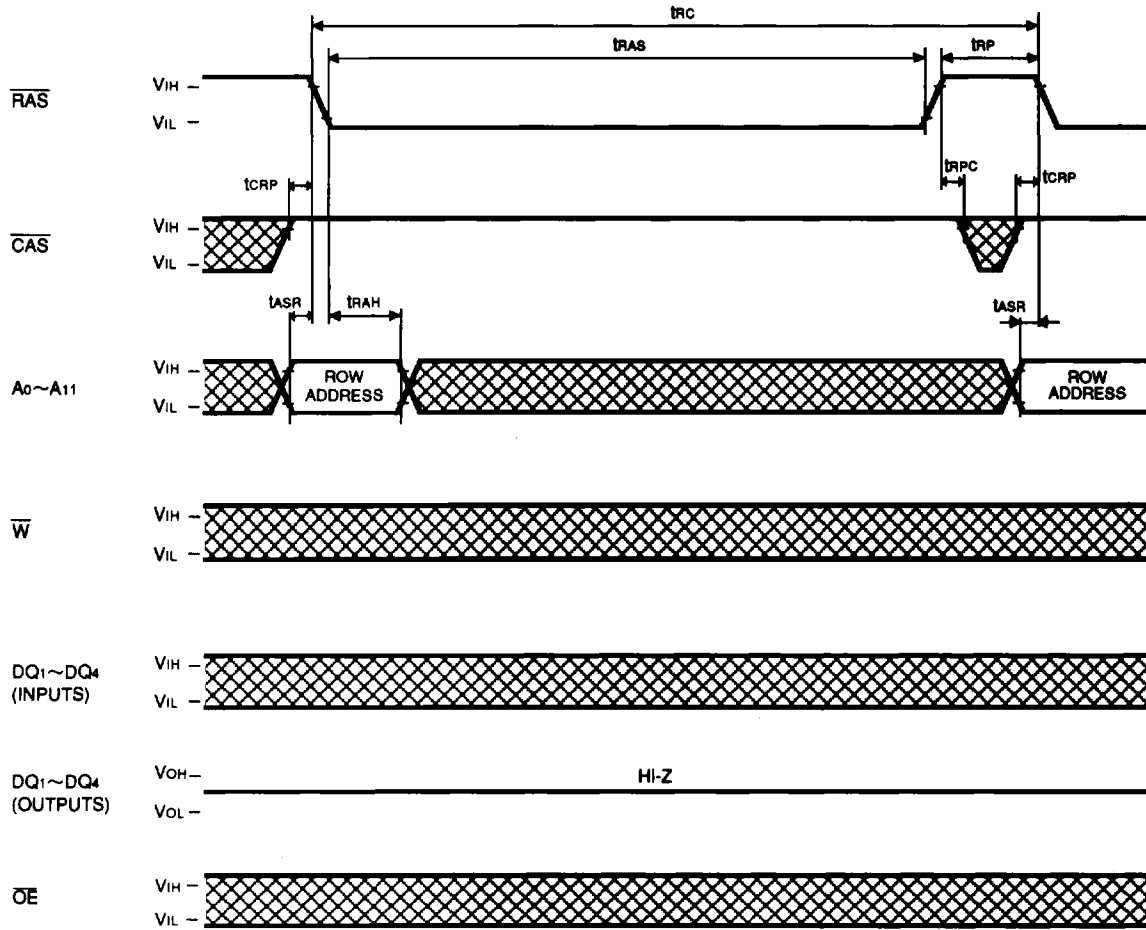## Write Cycle (Early write)
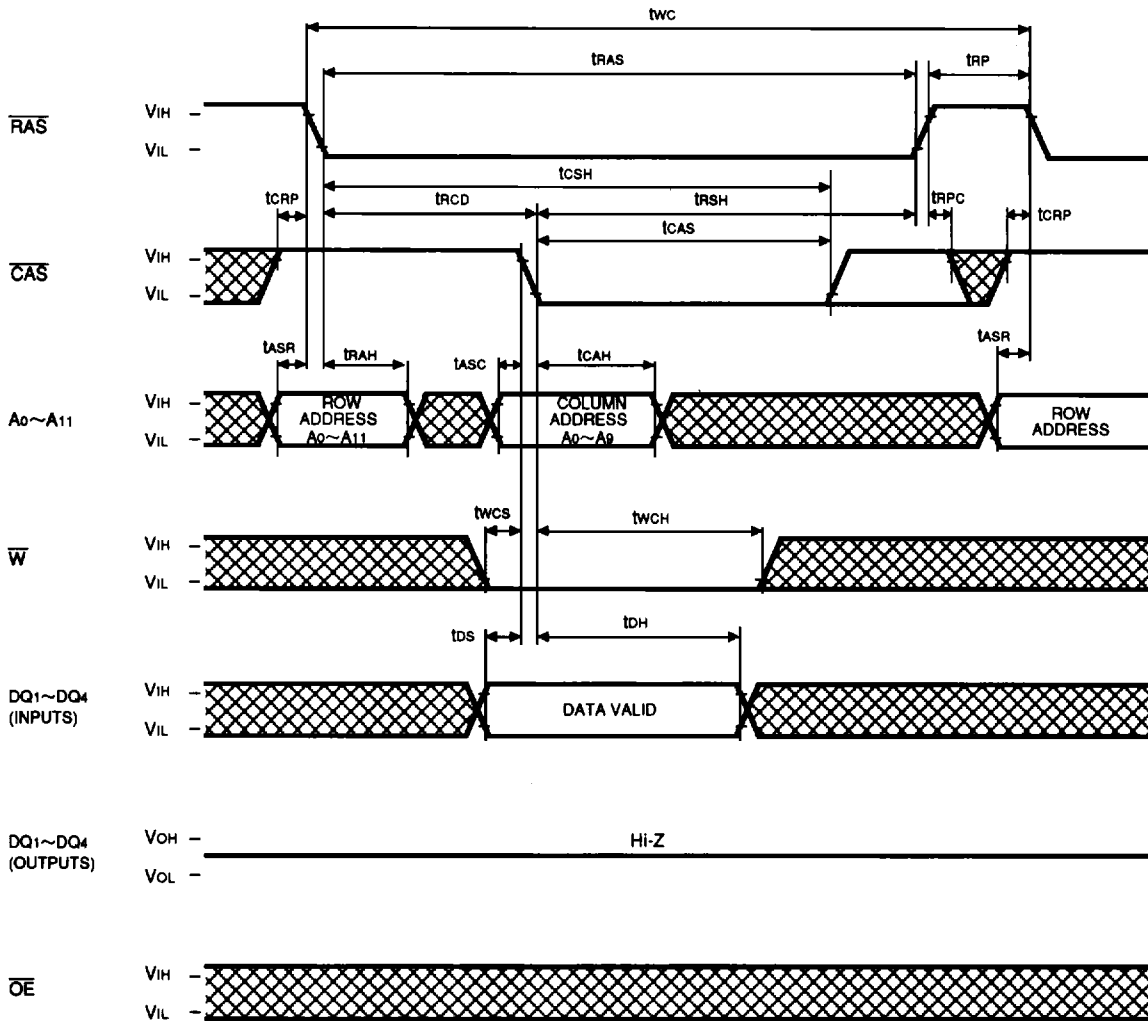
Write Cycle (Delayed write)

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Read-Write, Read-Modify-Write Cycle

$\overline{RAS}$-only Refresh Cycle

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$\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle
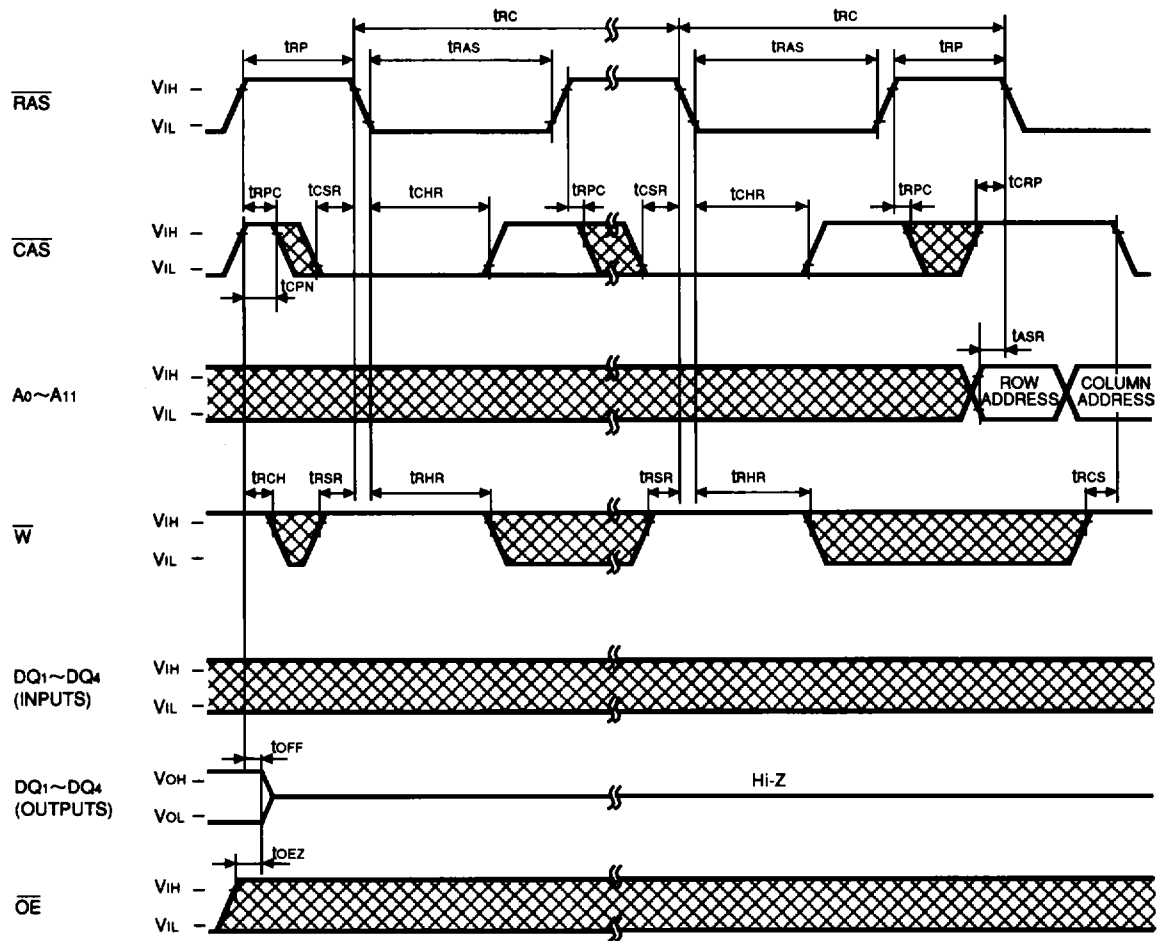
Hidden Refresh Cycle (Read) (Note 28)
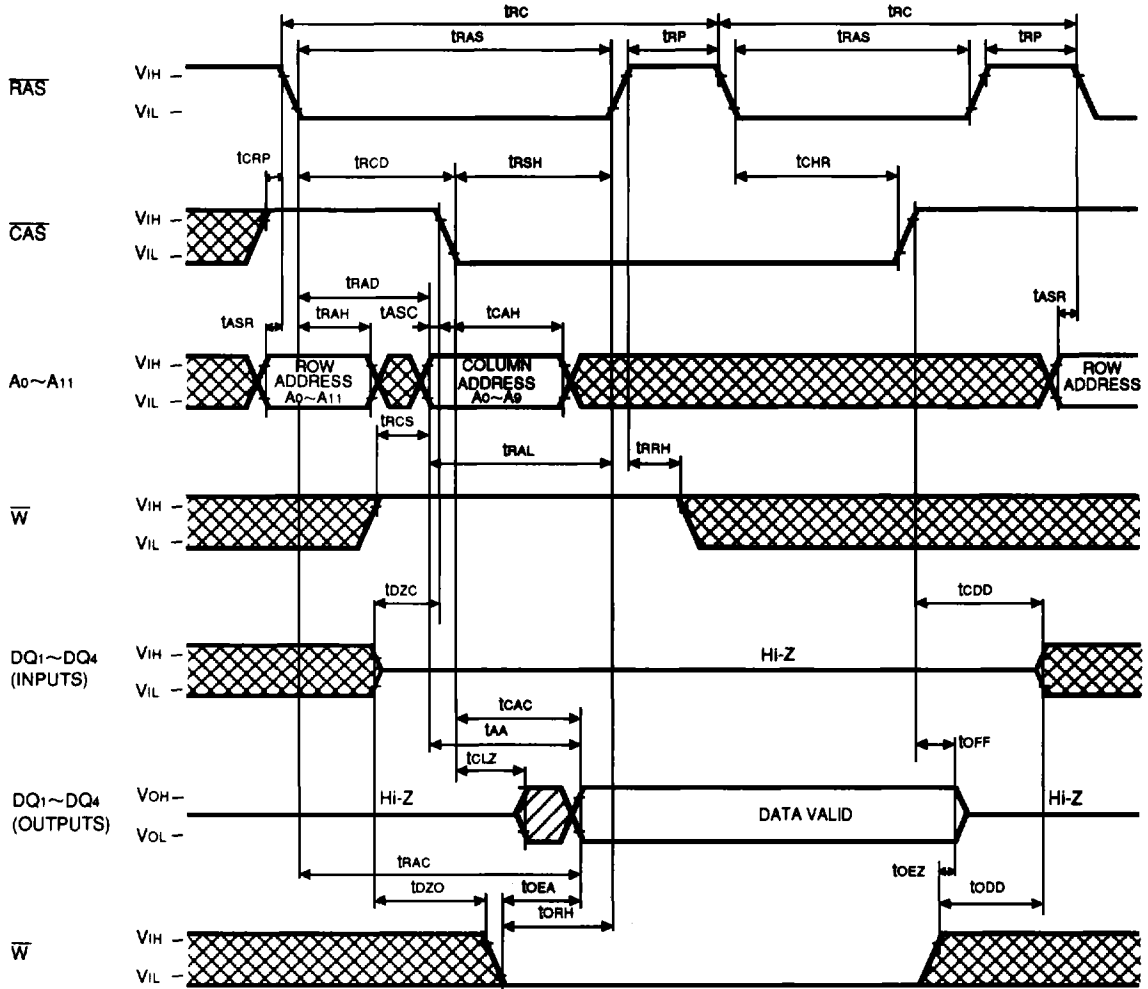
Note 28: Early write, delayed write, read write or read modify write cycle is applicable instead of read cycle.
Timing requirements and output state are the same as that of each cycle shown above.

MITSUBISHI ELECTRIC
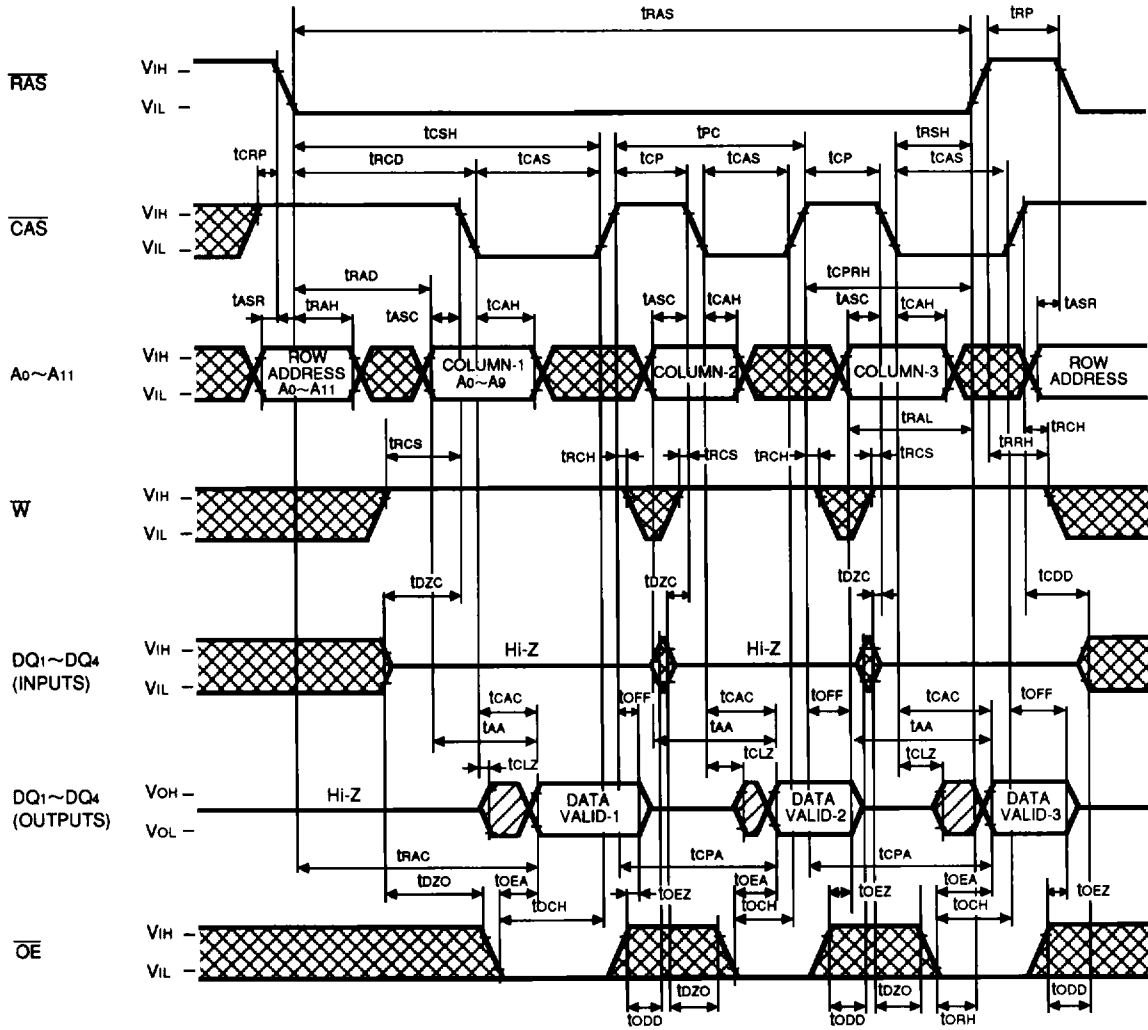
Fast Page Mode Read Cycle

Fast Page Mode Write Cycle (Early Write)

MITSUBISHI ELECTRIC
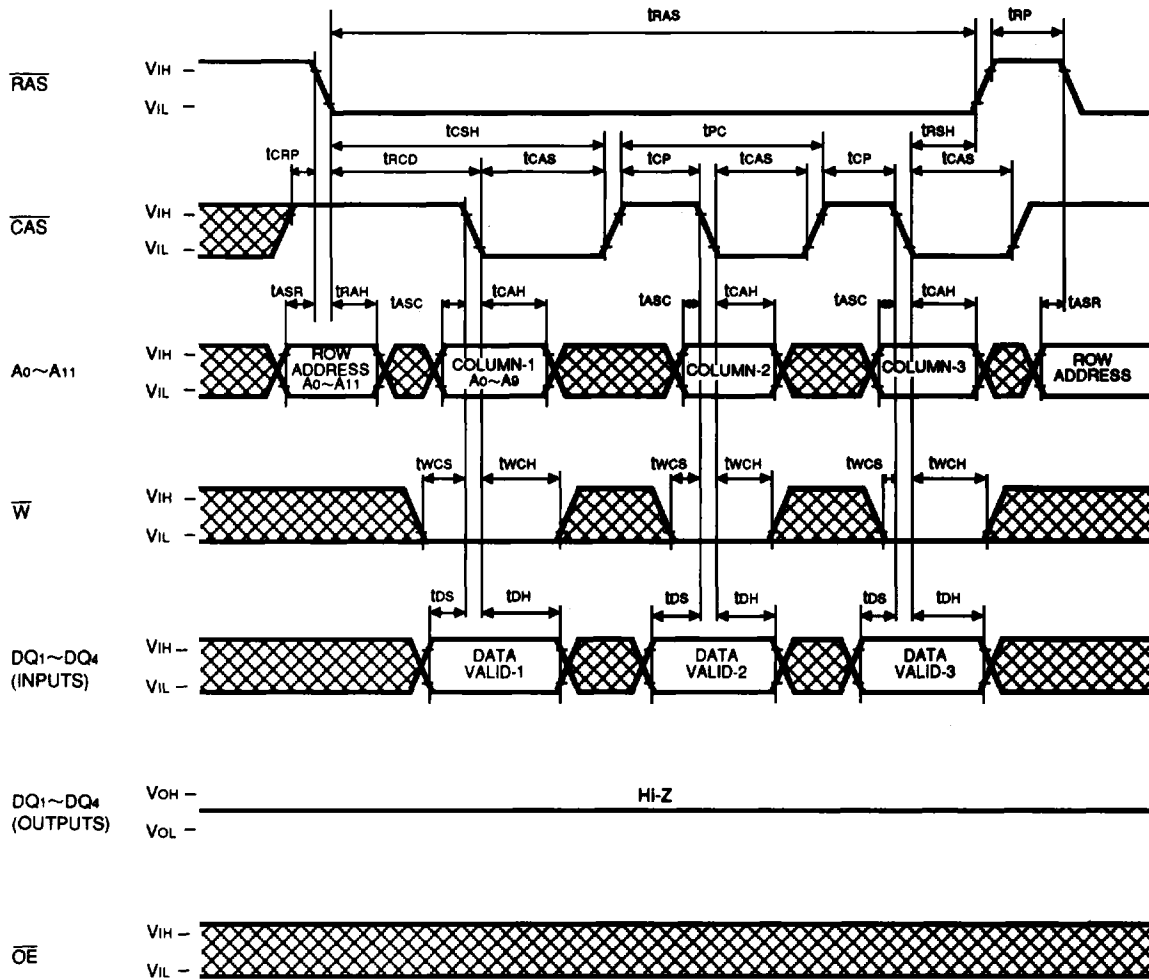
Fast-Page Mode Write Cycle (Delayed Write)
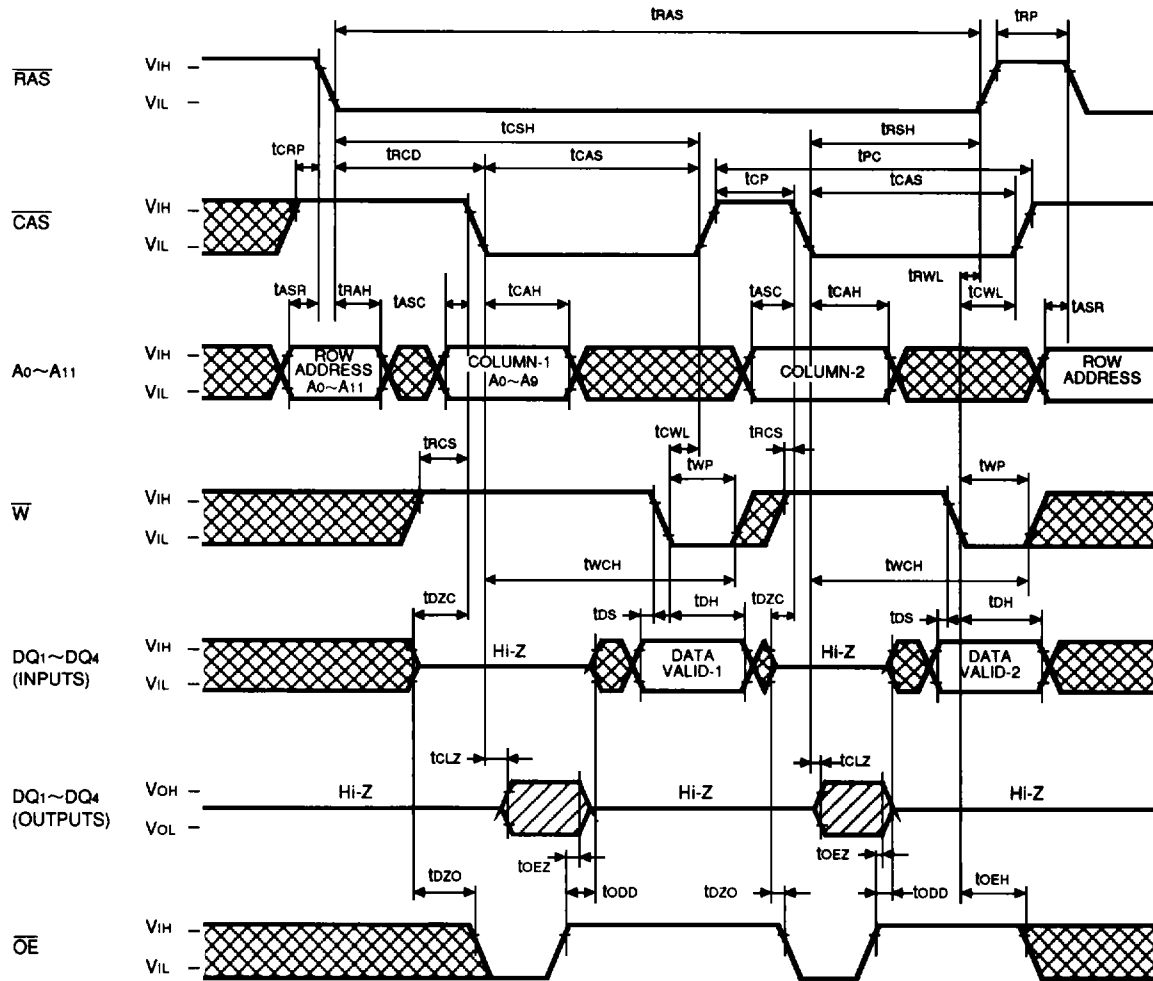
Fast Page Mode Read-Write, Read-Modify-Write Cycle
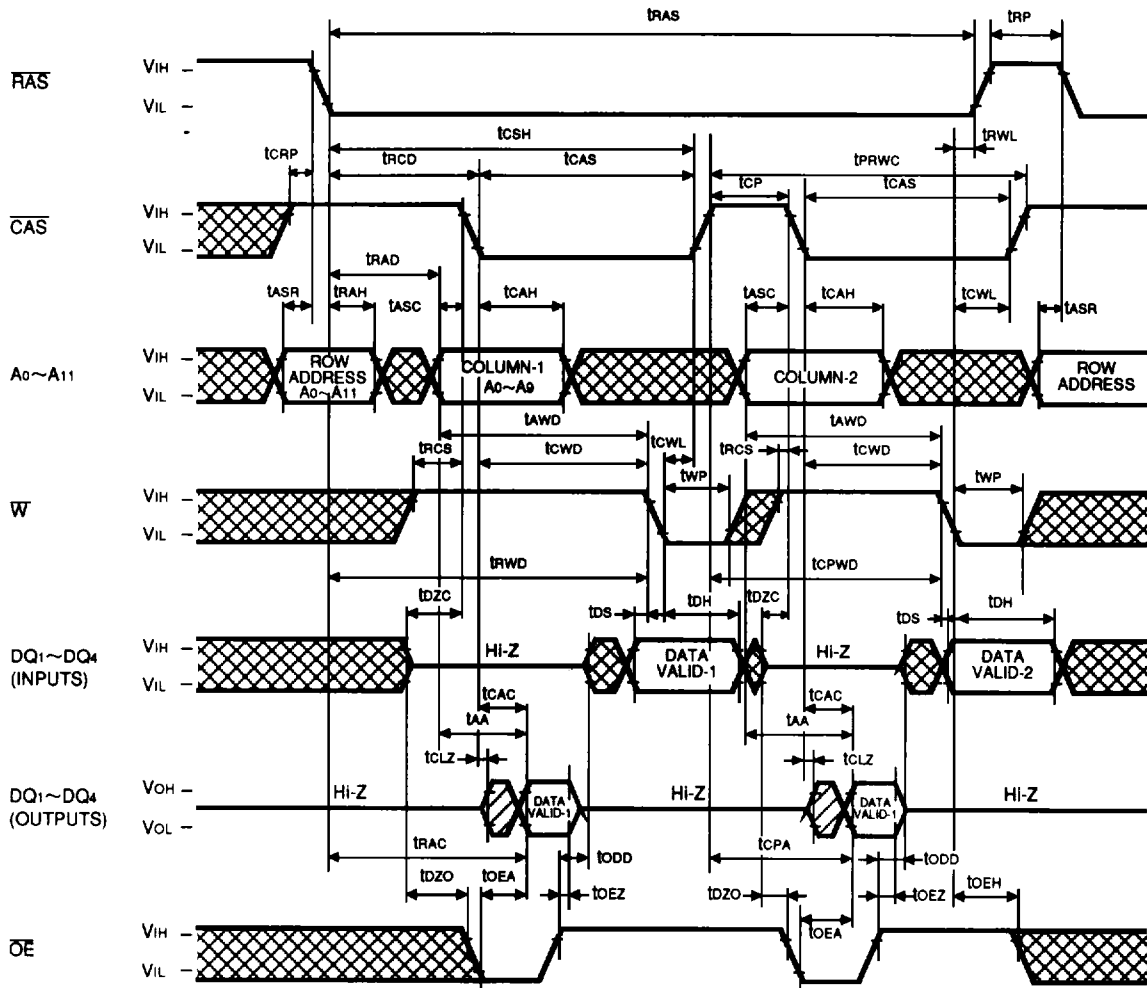
MITSUBISHI ELECTRIC

TEST Mode SET Cycle

Symbol	Parameter	Limits				Unit
		M5M417800A-6,-6S		M5M417800A-7,-7S		
		Min	Max	Min	Max	
twSR	$\overline{W}$ setup time before $\overline{RAS}$ low	10		10		ns
twHR	$\overline{W}$ hold time after $\overline{RAS}$ low	10		15		ns

Note 29 : The test mode function is initiated by a $\overline{W}$ and $\overline{CAS}$ before $\overline{RAS}$ cycle (WCBR cycle) as specified in timing diagram.
The test mode function is terminated by either a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR refresh cycle) or a $\overline{RAS}$ only refresh cycle.
During the test mode, the device is internally organized as 16 bits wide (1M bytes depth). No addressing of CA0, CA1 is required.
During a write cycle, data must be applied to all DQ (input) pins. The data can be different between DQ pins. The data on each DQ
pin is written into 2 bits memory cells, respectively. During a read cycle, each DQ (output) pin shows the test result of the 2 bits,
respectively. High state indicates that they are same. Low state indicates that they are not same.
During the test mode operation, WCBR cycle can be used to perform refresh.
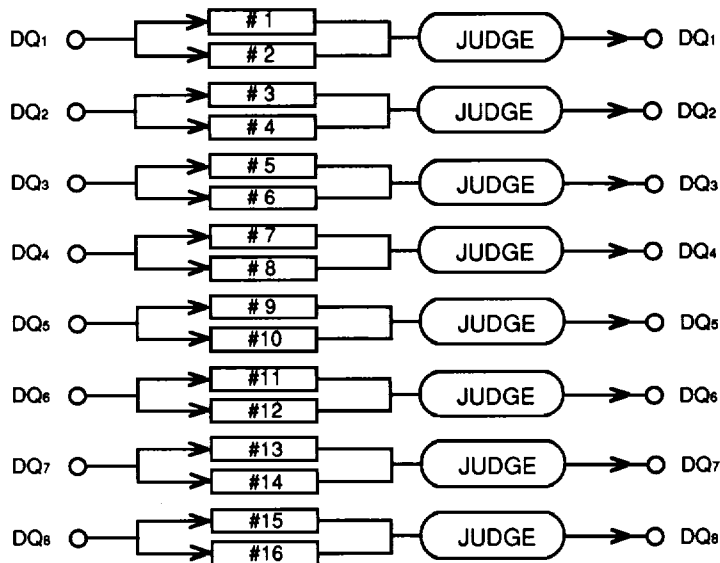
TEST Mode SET Cycle

MITSUBISHI
ELECTRIC
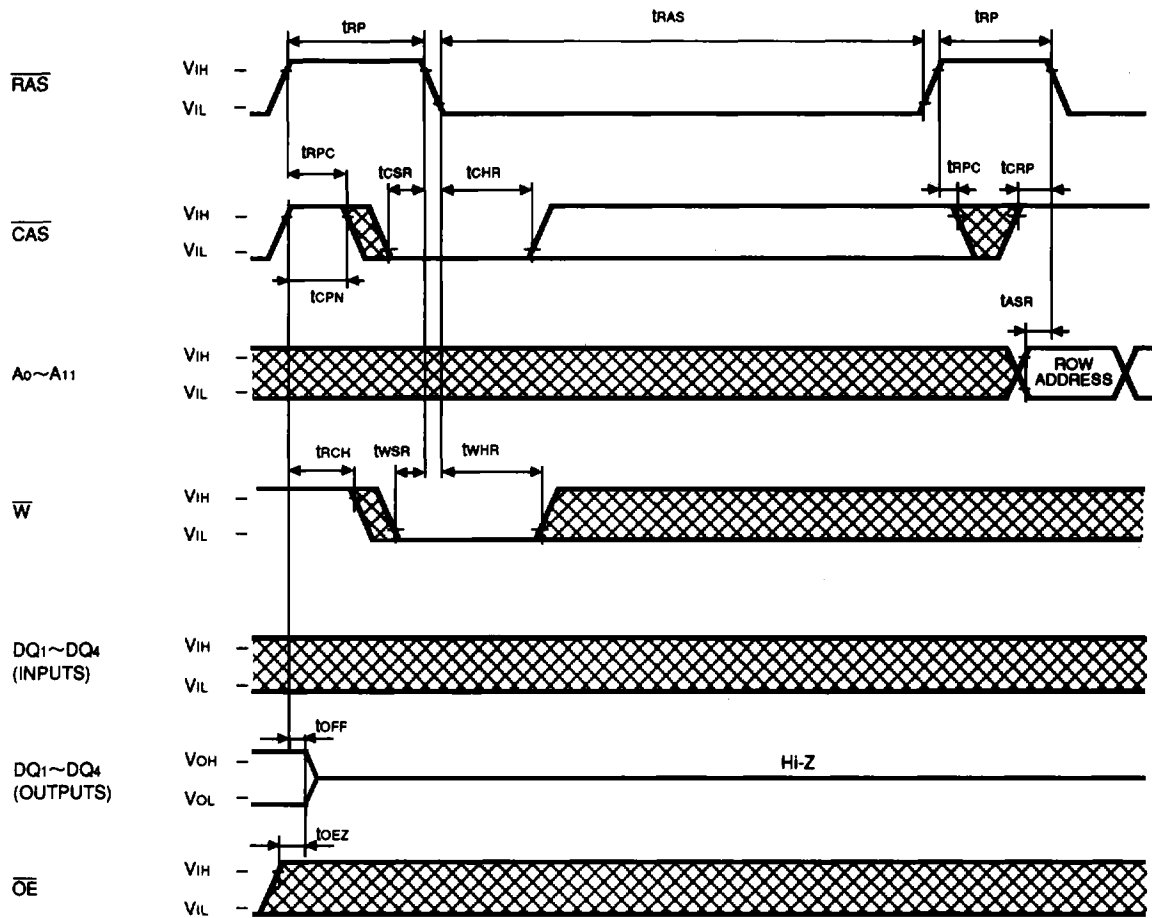
SELF REFRESH SPECIFICATIONS

Self refresh devices are denoted by "S" after speed item, like -6S / -7S. The other characteristics and requirements than the below are same as normal devices.

ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V±10%, Vss = 0V, unless otherwise noted) (Note 2)

| Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
Icc9 (AV)	Average supply current from Vcc Self-Refresh cycle	M5M417800A (S)	$\overline{RAS} = \overline{CAS} \leq 0.2V$			400	μA

TIMING REQUIREMENTS (Ta = 0~70℃, Vcc = 5V±10%, Vss = 0V, unless otherwise noted See notes 12,13)

Symbol	Parameter	Limits				Unit
		M5M417800A-6S		M5M417800A-7S		
		Min	Max	Min	Max	
tRASS	Self Refresh $\overline{RAS}$ low pulse width	100		100		μs
tRPS	Self Refresh $\overline{RAS}$ high precharge time	110		130		ns
tCHS	Self Refresh $\overline{RAS}$ hold time	-50		-50		ns
tRSR	Read setup time before $\overline{RAS}$ low	10		10		ns
tRHR	Read hold time after $\overline{RAS}$ low	10		15		ns

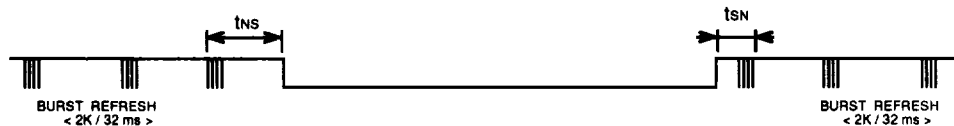## SELF REFRESH ENTRY & EXIT CONDITIONS

(1) In case of distributed refresh

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS} \leq 32$ ms and $t_{SN} \leq 32$ ms.
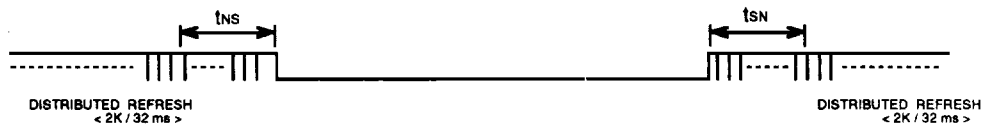
(2) In case of burst refresh

The last / first full refresh cycles (2K) must be made within t_{NS} / t_{SN} before / after self refresh, on the condition of $t_{NS} + t_{SN} \leq 32$ ms.

Self Refresh Cycle

MITSUBISHI ELECTRIC